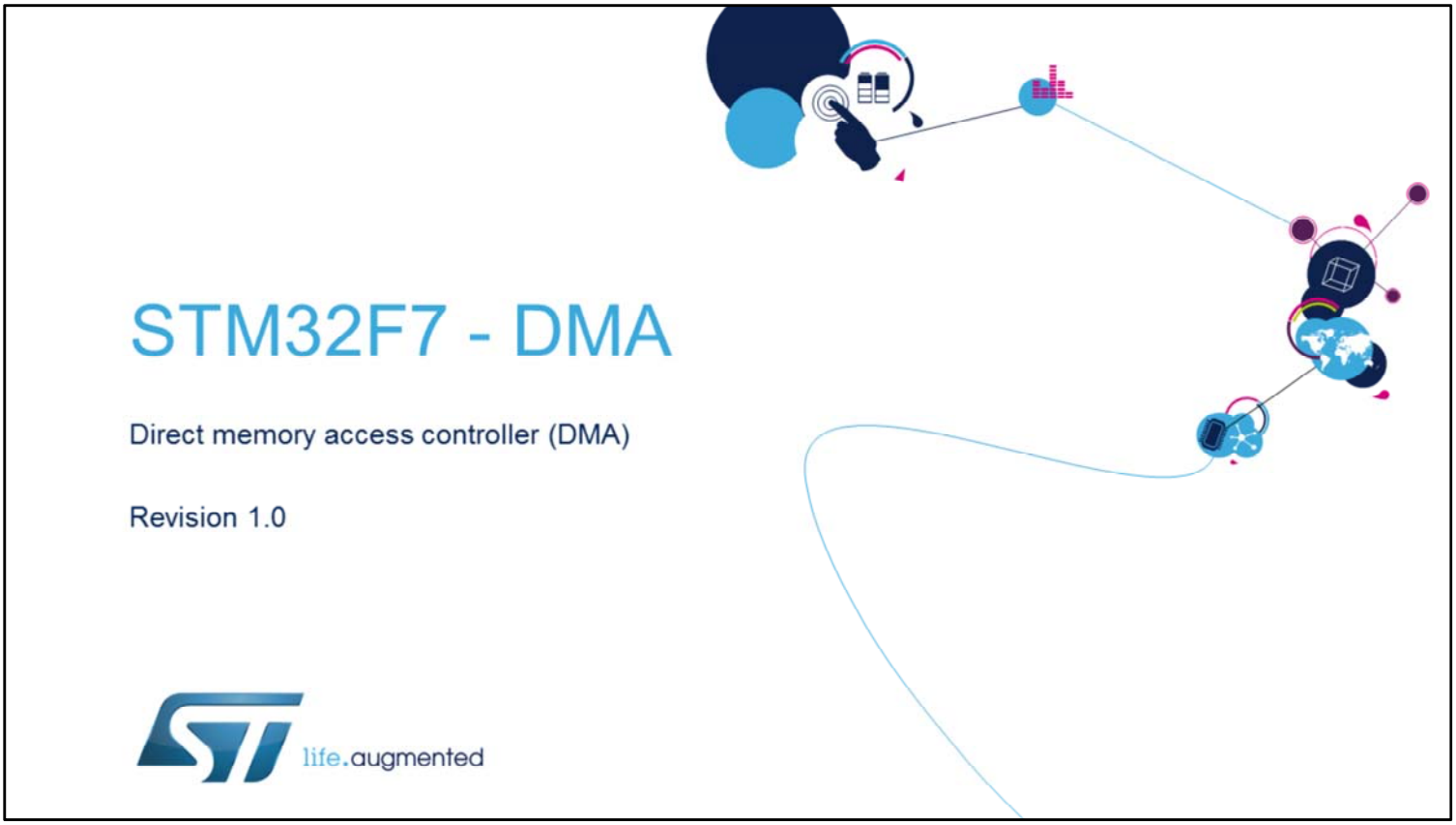
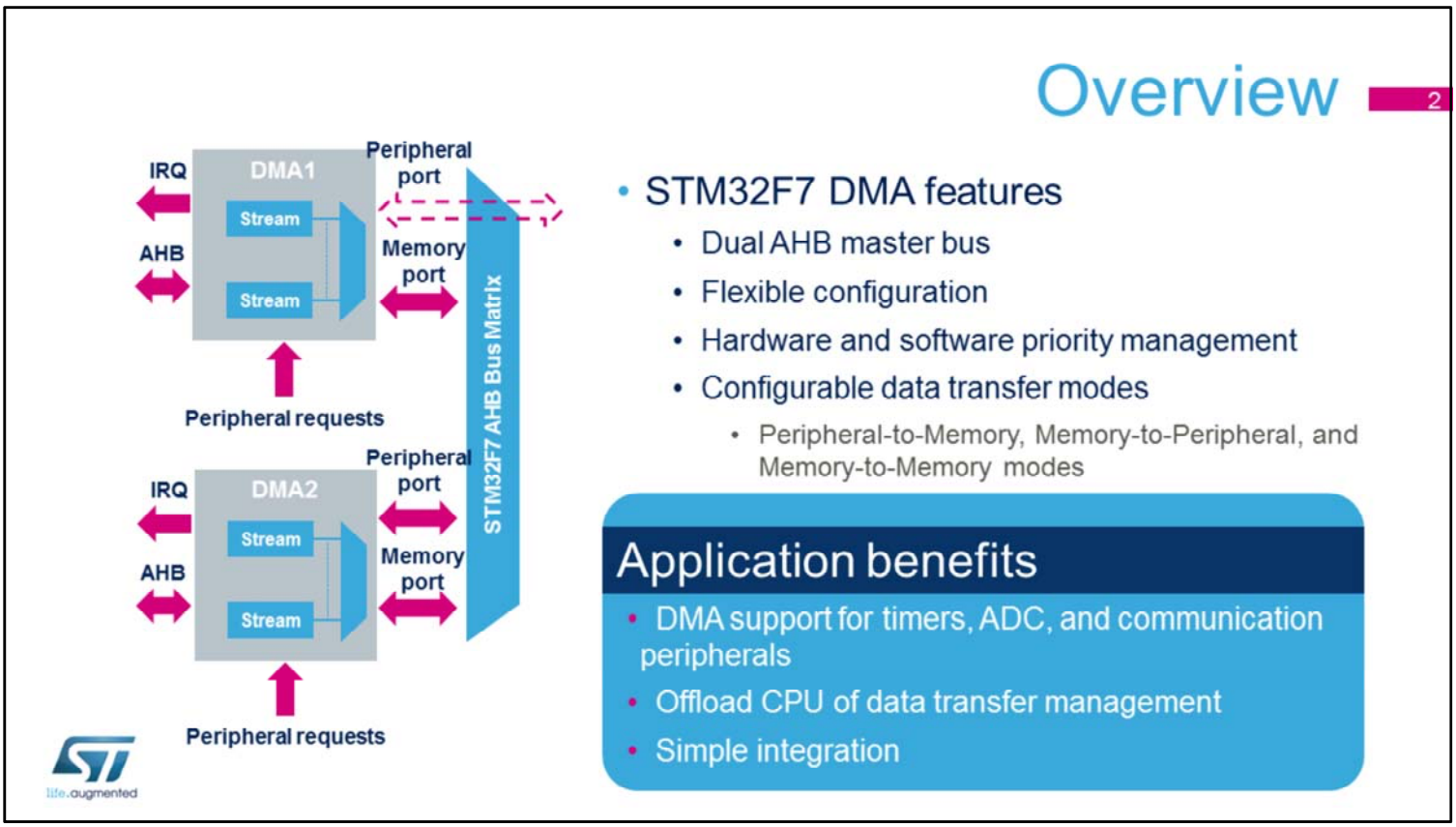
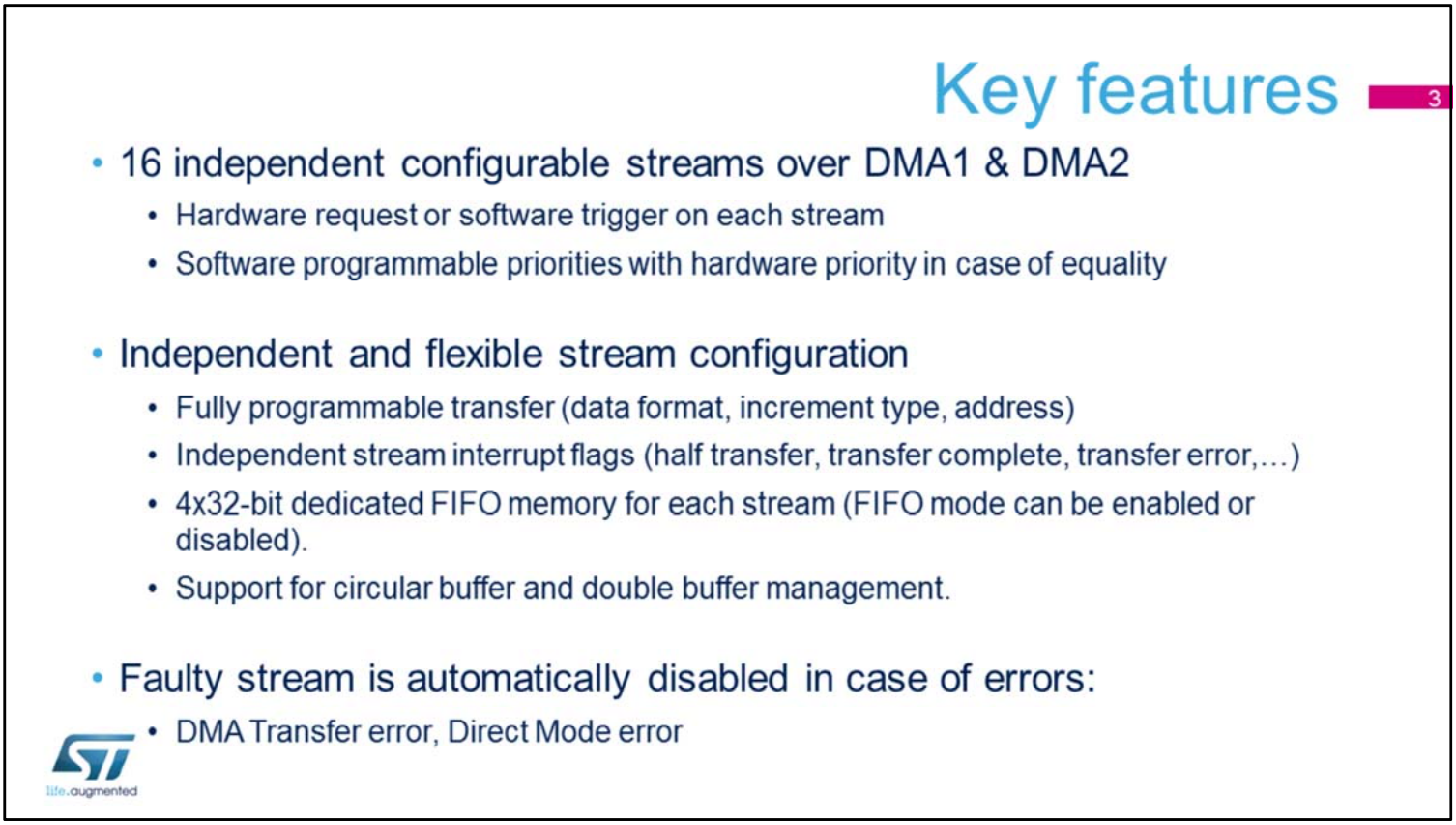


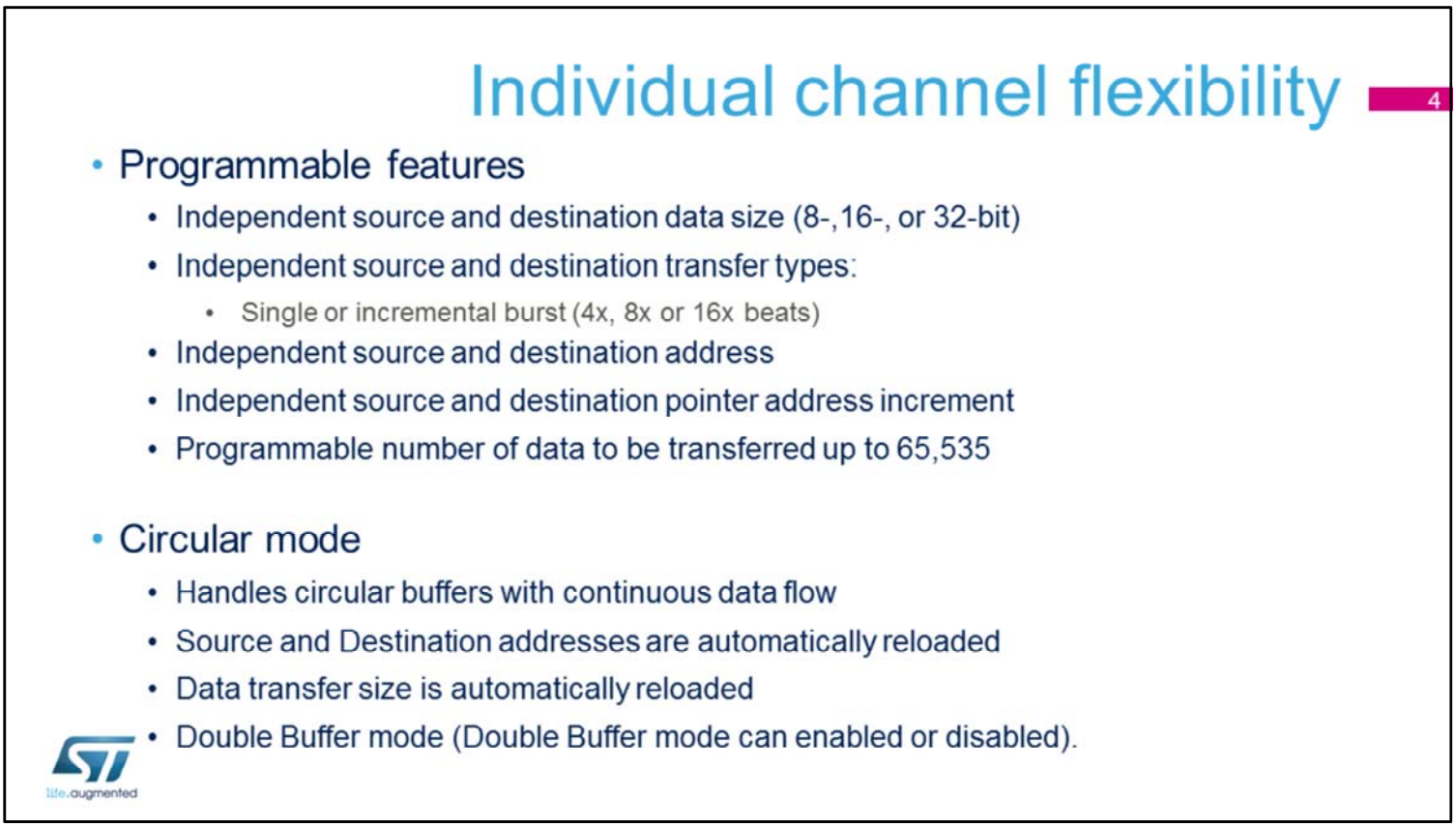
Welcome to this presentation of the STM32F7 direct memory access controller (DMA) . It covers the main features of this module, which is widely used to handle the STM32 peripheral data transfers.



The STM32F7 has two Direct Memory Access controllers designed to efficiently support data transfers from peripherals and memories without any loading of the CPU. The DMA controllers are fully configurable and manage hardware and software priorities between streams as well as data transfer modes.



The two DMA controllers (DMA1 and DMA2) have 16 streams in total, each dedicated to managing memory access requests from many peripherals. Each stream has flexible hardware requests and support for software triggers. The stream software priority is programmable and a hardware priority is used in case of equality. Streams are independently configurable. Each stream has its own data format, increment type and data address for both source and destination.
A four-word FIFO by stream allows to perform data packing/unpacking and burst transfers.
Independent stream interrupt flags allow to trigger half transfer, transfer complete, transfer error events. In case of a transfer error, the faulty stream is automatically disabled without any impact on the other active DMA streams.



For each stream, the source and destination data size format is independently configurable for 8-, 16- or 32-bit packets. The transfer type for the source and the destination can be programmed in single mode or in burst mode independently. The source and destination address and pointer increment is also independently configurable. The transfer data size can be pre-programmed up to 65535. Circular buffer mode is available to support a continuous flow of data. The source and the destination addresses and the number of data to be transferred are automatically reloaded after the complete transfer. Double Buffer mode allows the switching between two memory buffers to be managed by hardware.

Stream transfer management

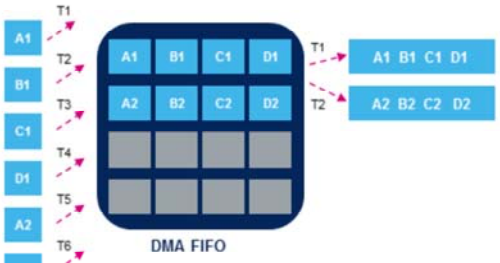
- Memory-to-Memory mode
  - Transfer starts as soon as the stream is enabled (No hardware request)
- Peripheral-to-Memory, Memory-to-Peripheral,
  - A transfer on DMA peripheral port occurs on each hardware request
  - Once the transfer is completed, the request is acknowledged

Memory-to-memory mode allows transfers from one address location to another without a hardware request. Once the stream is configured and enabled, the transfer starts immediately. When data is transferred to or from a peripheral, the hardware request coming from the selected peripheral is used to trigger the data transfer on DMA Peripheral port. Once the transfer is completed, the request is acknowledged.

FIFO: data packing/unpacking

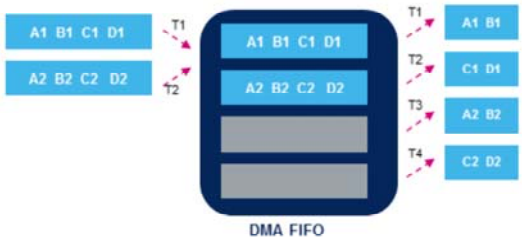
- Supported operations:
  - 8-bit / 16-bit → 32-bit / 16-bit (Packing)
  - 32-bit / 16-bit → 8-bit / 16-bit (Unpacking)

Data packing example (8-bit → 32-bit)



- Source data width = 8-bit
- Destination data width = 32-bit
- 8 transfers are performed from source to DMA FIFO.
- 2 transfers are performed from DMA FIFO to destination.

Data unpacking example (32-bit → 16-bit)



- Source data width = 32-bit
- Destination data width = 16-bit
- 2 transfers are performed from source to DMA FIFO.
- 4 transfers are performed from DMA FIFO to destination.

life.augmented

When FIFO mode is enabled (Direct mode disabled) the DMA controller manages the data format difference between source and destination (data packing and unpacking). thanks to its internal FIFO, the DMA stream can reduce software overhead and the number of transactions over the AHB Bus.

FIFO: Threshold levels & Burst mode

- Threshold level triggers the data transfers to/from memory.
- Each stream has independent configurable threshold levels:
  - Four threshold levels available : ¼ FIFO Full , ½ FIFO Full, ¾ FIFO Full, and FIFO Full
- Burst mode:
  - Burst mode is available only when FIFO mode is enabled (Direct mode disabled)
  - Available Burst modes:
    - INC4: 1 burst = 4 beats (4 Words, 8 Half-Words or 16 Bytes)
    - INC8: 1 burst = 8 beats (8 Half-Words or 16 Bytes)
    - INC16: 1 burst = 16 beats (16 Bytes)

FIFO threshold should be compatible with Burst size:

Memory data size	Burst Size	Allowed threshold levels
Byte	4 Beats (INC4)	¼, ½, ¾ and Full
	8 Beats (INC8)	½ & Full
	16 Beats (INC16)	Full
Half-Word	4 Beats (INC4)	½ & Full
	8 Beats (INC8)	Full
Word	4 Beats (INC4)	Full

In burst mode or in single mode, the FIFO threshold level determines when the data in the FIFO should be transferred to/from memory.

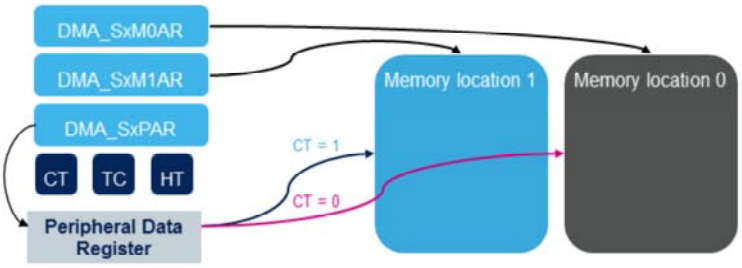
There are four configurable threshold levels per stream starting from “one quarter FIFO Full” to “FIFO Full”. Depending on the transfer direction on the memory port, when the FIFO threshold is reached, the FIFO is filled from or flushed to the memory location.

Burst mode is only available when FIFO mode is enabled. When setting burst mode, the FIFO threshold should be compatible with burst size. It allows the DMA streams to have the burst data available in the FIFO to carry out a burst transfer.

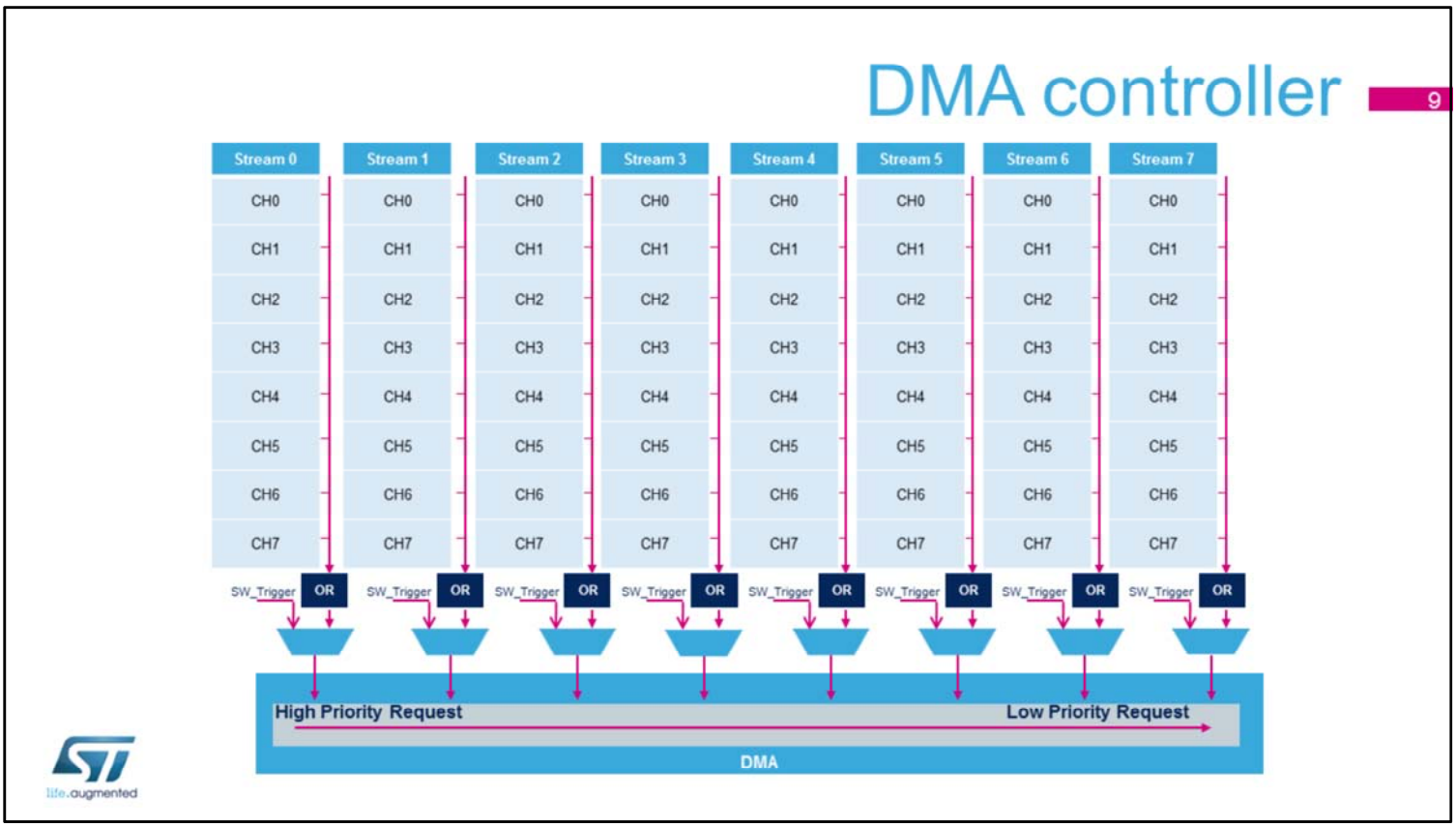
Circular & double buffer modes

8

- Circular mode:
  - All FIFO features and DMA events (TC, HT, TE) are available in this mode.
  - The number of data items is automatically reloaded and the transfer restarted.
  - This mode is NOT available for Memory-to-Memory transfers.
- Double Buffer mode: (circular mode only)
  - Two memory address registers are available (DMA_SxM0AR & DMA_SxM1AR)
  - Allows the switching between two memory buffers to be managed by hardware.
  - Memory-to-Memory mode is not allowed
  - A flag & control bit (CT) is available to monitor which destination is being used for data transfer.
  - TC flag is set when transfer to memory location 0 or 1 is complete.



DMA controllers support Circular mode allowing to configure the number of data items to transfer once, and automatically restart the transfer after a Transfer Complete event. Double buffer mode is only available in Circular mode. It allows to switch automatically by hardware between two memory addresses each time a Transfer Complete event occurs. In double buffer mode, a status flag and control bit (CT) is available to monitor which destination is being used for data transfers.



The DMA controller provides access to 8 streams with multiple channels per stream depending on the device part number. For example up to 8 channels are available on STM32F74xx microcontrollers. Each stream channel is connected to only one peripheral request. A peripheral request can be connected to different streams to guarantee more flexibility during configuration.
A channel request multiplexer allows to have only one channel active per stream. Software must ensure that a peripheral request is enabled only on one stream.

Software triggers available on DMA2 can only perform memory-to-memory transfers.

Interrupts

- Interrupt events for each channel

Interrupt event	Description
Half transfer	Set when half of the data transfer size has completed
Transfer complete	Set when the full data transfer size has completed
Transfer error	Set when a bus error occurs during the data transfer
FIFO Error	Set when FIFO underrun/overrun condition or Threshold-burst size incompatibility
Direct Mode Error	Is available only in: Peripheral-to-Memory mode, in Direct mode, when Memory Incrementation is disabled. Indicates that new data is being transferred to a memory location whereas the previous transfer is not yet completed.

Each DMA stream is designed with this group of interrupt events. The Half Transfer interrupt flag is set when half the data has been transferred; the Transfer Complete flag is set when the transfer is complete; the Transfer Error flag is set when an error occurs during the data transfer; the FIFO Error flag is set whenever a DMA FIFO underrun/overrun condition is detected or Threshold-burst size incompatibility; the Direct Mode Error flag is set in Peripheral-to-Memory mode, in Direct mode, when Memory Incrementation is disabled. It indicates that new data is being transferred to a memory location whereas the previous transfer is not complete yet.

DMA in low-power modes

Mode	Description
Run	Active.
Sleep	Active. DMA interrupts can wake the STM32F7.
Stop	Frozen. DMA registers content is retained.
Standby	Powered-down. DMA must be reinitialized after exiting Standby mode.

The DMA is active in Run and Sleep modes. DMA interrupts will wake the STM32F7 from Sleep mode. In Stop mode, the DMA is stopped and the contents of the DMA registers are retained. The DMA is powered-down in Standby mode, and the DMA registers must be reinitialized after exiting Standby mode.

References

- For more details and additional information, refer to the following:
  - Application note AN4031: Using the STM32F2 and STM32F4 DMA controller

For more details, please refer to the following documentation available on our website.